Ordering number: EN ※4302

SANYO No.※4302

LC86P6232

CMOS LSI

8-Bit Single Chip Microcomputer

Preliminary

Overview

The LC86P6232 microcomputer is CMOS 8-bit single chip microcomputer with one-time PROM for LC866200A series.

This microcomputer has the function and the pin discription of LC866200A series mask ROM version, and 32K-byte PROM.

QFP package is available for shipping as well as LC866200A series. It is suitable to set up first release, prototyping, developing and testing of set.

Features

(1) Option switching by PROM data

The option function of LC866200A series can be specified by PROM data.

LC86P6232 can be checked the functions of trial piece using mass production board.

(2) Internal 32K-byte PROM

32K-byte PROM is built in. This corresponds to LC866232A/28A/24A/20A/16A.

(3) The pin and package compatible with mask ROM version

(4) The characteristics compatible with mask ROM version

(5) Factory shipment

QFP-100E

Programming service

We offers verious services at nominal charges. These include ROM writing, ROM reading, and package stamping and screening. Contact your local our representative for further information.

Notice for use

LC86P6232 is provided for the first release and small shipping of LC866200A series.

At using, take notice of the followings.

(1) Reset

It is necessary to be sure to go into 'L' level and hold for 200 μs to reset terminal after power supplied voltage has been over inferior limit of supply voltage.

The option is specified until 3m s after going into 'H' level to reset terminal by degrees.

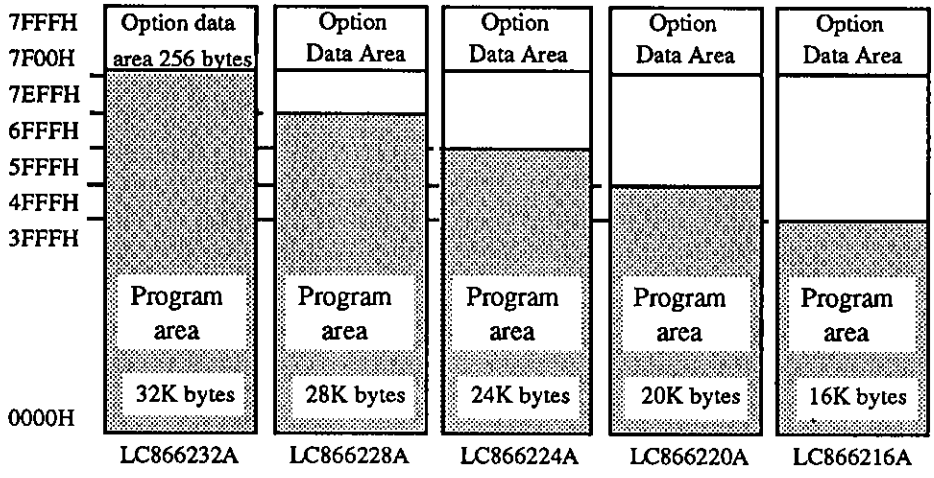
The program is executed from 0H of program counter. The output form of all ports are N-channel open drain while 'L' level to reset terminal.

(2) Option

LC86P6232 uses 256 bytes which is addressed on 7F00H~7FFFH in the program memory as option data area. This area does not affect the execution of program but the program memory capacity of LC866232A is 32512 bytes which is addressed on 0000H ~ 7EFFH.

The option data is created by option specified program "SU866200. EXE". The created option data is linked program area by linkage loader "L866200. EXE".

(3) ROM space

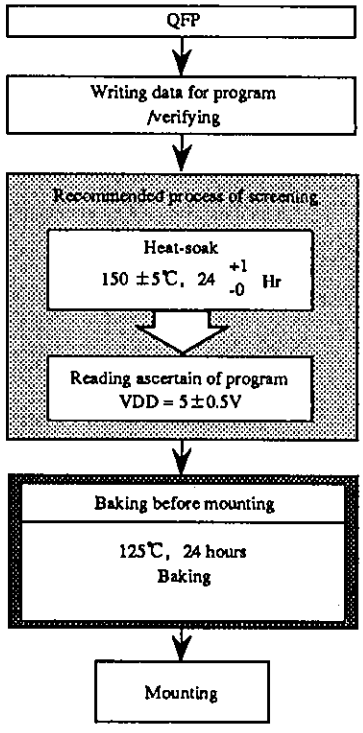


(4) Ordering information

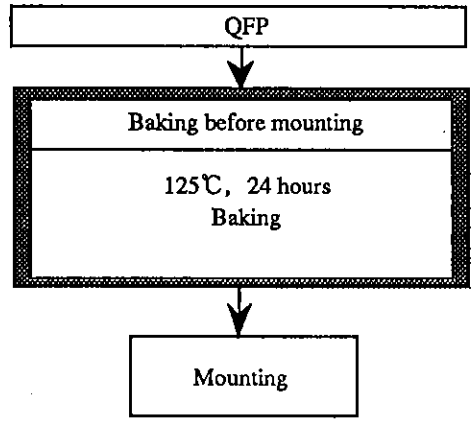
- When ordering identical mask ROM and PROM devices simultaneously.
  Provide an EPROM containing the target memory contents together with separate order forms for each of the mask ROM and PROM versions.
- When ordering a PRON device.
  Provide an EPRON containing the target memory contents together with an order form.

(5) Condition of Pre-mounting

a. Shipping with a blank PROM (Programming the data by yourself)
This microcomputer is provided QFP package, but the condition before mounting is not equal. The following is the procedure of mounting.



b. Shipping with a programmed PROM (Programming the data by Sanyo)



[Notes] · The baking must be done before mounting the QFP on the substrate (This baking is called pre-baking). After pre-baking, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30℃ or less and a humidity level of 70% or less. Please solder within eight hours.

· It is not possible to perform a write test on the blank PROM. 100% yeild, therefore, cannot be guaranteed.

(6) Points of difference LC86P6232 and LC866200A series

Item	LC86P6232	LC866232A/28A/24A/20A/16A
Operating temperature range (Topg)	-30℃～70℃	-30℃～70℃
Output form of port at reset	Open drain output	Output form specified by option data
Output form of segment	Pulldown resistor	Pulldown resistor : Provided / Not provided
·S0/T0～S6/T6	Not provided	Specified by option
·S7/T7～S15/T15	Provided (fixed)	Provided (fixed)
·S16～S23	Provided (fixed)	Specified by option
·S24～S31	Provided (fixed)	Specified by option
Operating supply voltage range (VDD)	4.5～6.0V	2.5～6.0V

Option

· A kind of option corresponding LC86P6232

A kind of option	Pins, Circuits	Contents of option
Input/output form of input/output ports	Port 0 (specified in a bit)	1. Input : No Pullup MOS Tr. Output : N-channel open drain 2. Input : Pullup MOS Tr. Output : CMOS
	Ports 1, 2 (specified in a bit)	1. Input : Programmable pullup MOS Tr. Ouptu : N-channel open drain 2. Input : Programmable pullup MOS Tr. Output : CMOS
	Ports 3, 4, 5 (specified in a bit)	1. Input : No Programmable pullup MOS Tr. Ouptu : N-channel open drain 2. Input : Programmable pullup MOS Tr. Output : CMOS
Pullup MOS Tr. of input port	Port 7 (specified in a bit)	1. No pullup MOS Tr. 2. Pullup MOS Tr.

How to use

(1) Specification of option

LC86P6232 is programmed after specifying option data. The option is specified by SU866200. EXE. The specified option file and the file created by our macro assembler (M866200. EXE) are linked by our linker (L866200.EXE) which creates .HEX file, then the option code is put in the option specified area (7F00H～7FFFH) of its .HEX file.

(2) How to program for EPROM

LC86P6232 can be programmed by EPROM programmer with attachment ; W86EP6232Q.

· Recommended EPROM programmer

Productor	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL1890A

· "27512 (Vpp=12.5V) Intel high speed programming" mode available. The address must be set "0H～7FFFH" and jumper (DASEC) must be set 'OFF' at programming.

(3) How to use the data security function

"Data security" is the function disable to read the data of EPROM.

The following is the process in order to execute data security.

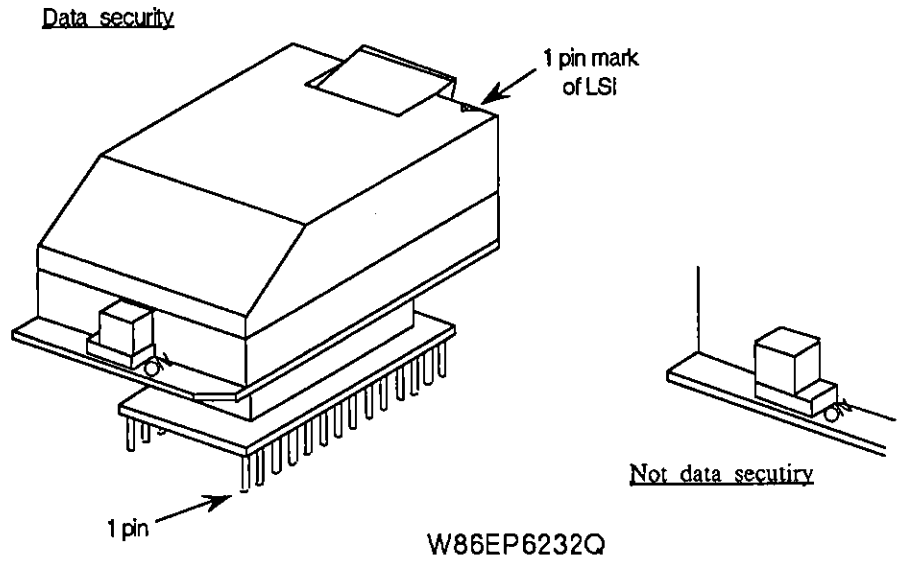
1. Set 'ON' the jumper of attachment.
2. Program again. Then EPROM programmer displays error. The error is the reason of data security, not trouble EPROM programmer or LSI.

Notes

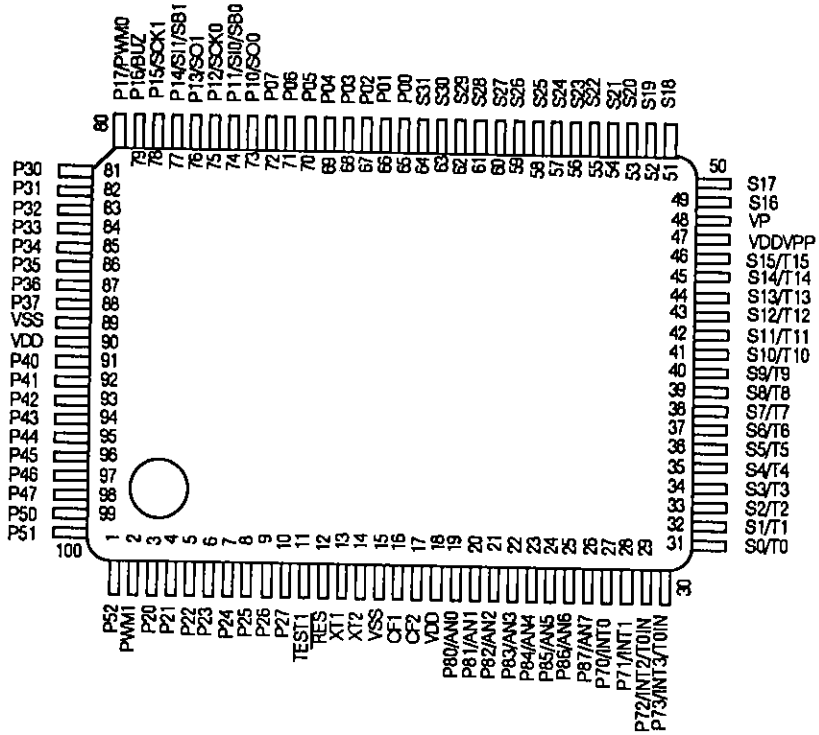
· Data security is not executed when the data of all address have 'FF' at sequence 2 above.

· The programming by sequential operation "BLANK→PROGRAM→VERIFY" cannot be executed data security at sequence 2 above.

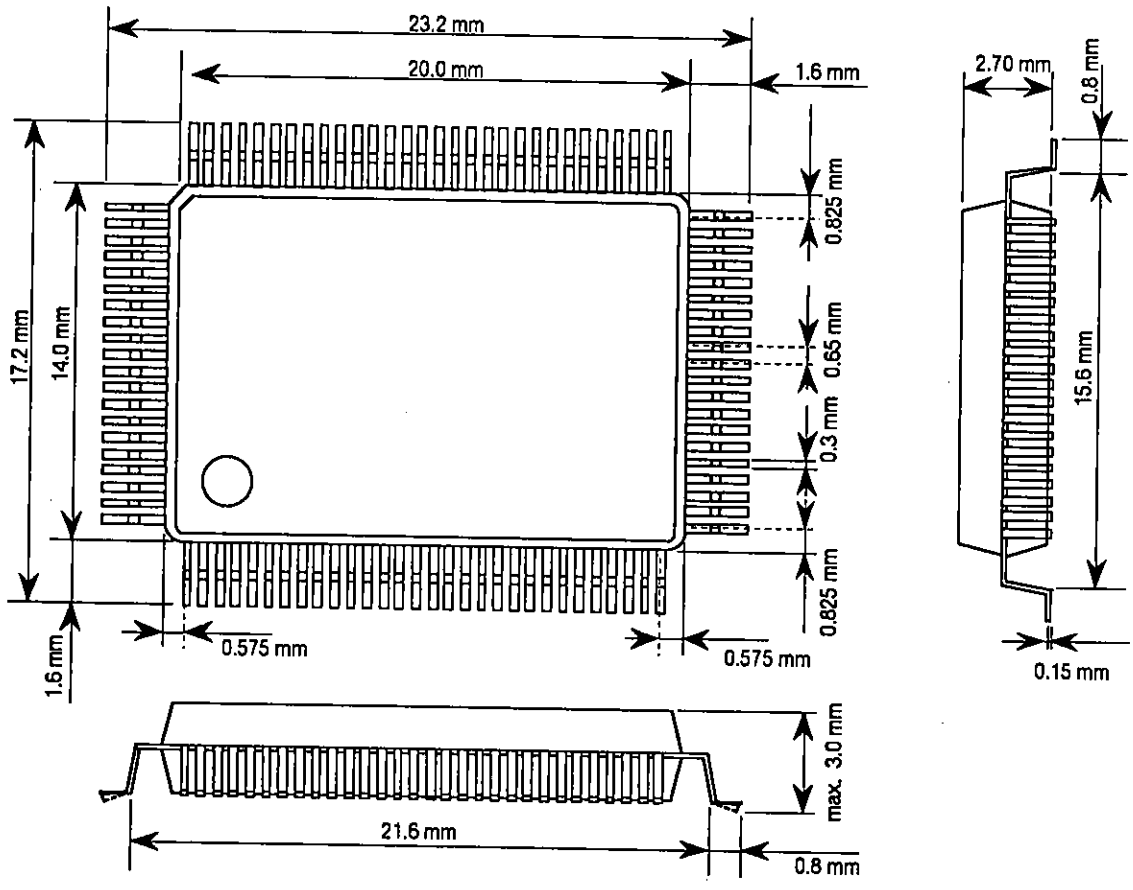
· Set 'OFF' the jumper after execution of data security.



Pin Assignment



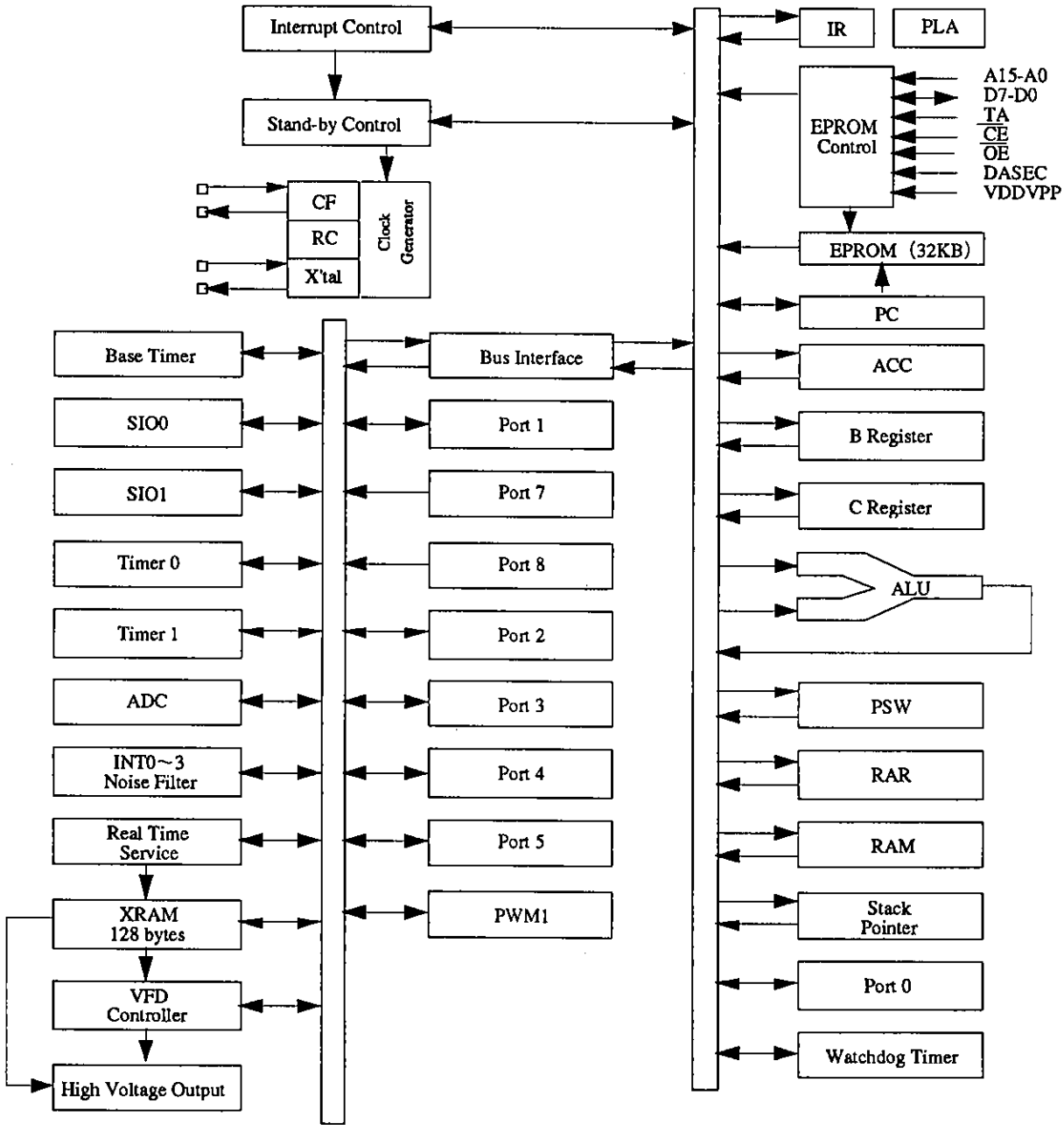
Package Dimensions 3151



SANYO : QIP100E

Notes · The baking must be done before mounting the QFP on the substrate (This baking is called pre-baking). After pre-baking, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30℃ or less and a humidity level of 70% or less. Please solder within eight hours.

System Block Diagram



LC86P6232 Pin description

Pin name	I/O	Function description	Option	Fumction at PROM mode
VSS		Power pin(-).		
VDD		Power pin(+).		
VP		Power pin(-) for VFD output pulldown resistor.		
VDDVPP		Power pin(+).		Power for programming
PORT0 P00～P07	I/O	·8-bit input/output port. ·Input for port 0 interrupt. ·Input/output in nibble units. ·Input for HOLD release.	·Pullup resistor : Provided / Not provided. ·Output form : CMOS/ N-channel open drain.	
PORT1 P10～P17	I/O	·8-bit input/output port. ·Input/output can be specified in bit unit. ·Other pin functions P10 : SIO0 data output P11 : SIO0 data input / bus input/output P12 : SIO0 clock input/output P13 : SIO1 data output P14 : SIO1 data input / bus input/output P15 : SIO1 clock input/output P16 : Buzzer output P17 : Timer 1 output (PWM output)	Output form : CMOS/ N-channel open drain.	Data input/output · D0～D7
PORT2 P20～P27	I/O	·8-bit input/output port. ·Input/output can be specified in bit unit.	·Pullup resistor : Provided / Not provided.	
PORT3 P30～P37	I/O	·8-bit input/output port. ·Input/output can be specified in bit unit. ·15v withstand voltage at N-channel open drain output.		Address input · A7～A0
PORT4 P40～P47	I/O	·8-bit input/output port. ·Input/output can be specified in bit unit. ·15v withstand voltage at N-channel open drain output.		Address input · A14～A8 · *P47 : TA (*4)*
PORT5 P50～P52	I/O	·3-bit input/output port. ·Input/output can be specified in bit unit. ·15v withstand voltage at N-channel open drain output.		
PORT7 P70 P71～P73	 I/O I	·4-bit input port. ·Other pin functions. P70 : INT0 input/HOLD release /N-channel Tr. output for watchdog timer. P71 : INT 1 input/HOLD release. P72 : INT 2 input/timer 0 event input. P73 : INT 3 input with noise filter/timer 0 event input. ·Interrupt received form, vector address.	Pullup resistor : Provided / Not provided.	 Input of PROM control signal · *DASEC (*1)* · $\overline{OE}$ *(*2)* · $\overline{CE}$ *(*3)*

	Leading	Trailing	Leading & Trailing	HIGH Level	LOW Level	VECTOR
INT0	○	○	×	○	○	03H
INT1	○	○	×	○	○	0BH
INT2	○	○	○	×	×	13H
INT3	○	○	○	×	×	1BH

Pin name	I/O	Function description	Option	Function at PROM mode
PORT8 P80～P87	I	·8-bit input port. ·Other functions. AD input port (8 port pins)		
PWM1	O	PWM output port (CMOS)		
S0/T0～ S6/T6	O	Output for VFD display controller segment/timing in common.		
S7/T7～ S15/T15	O	Output for VFD display controller segment/timing with internal pulldown resistor in common.		
S16～S23	O	Output for VFD display controller segment output internal pulldown resistor output		
S24～S31	O	Output for VFD display controller segment output internal pulldown resistor output		
$\overline{\text{RES}}$	I	Reset pin.		
TEST1	O	Test pin. Should be left unconnected.		
XT1	I	Input pin for 32.768kHz crystal oscillation. In case of non use, connect to VDD.		
XT2	O	Output pin for 32.768kHz crystal oscillation. In case of non use, should be left unconnected.		
CF1	I	Input pin for ceramic resonator oscillation.		
CF2	O	Output pin for ceramic resonator oscillation.		

*1 Memory select input for data security

*2 Output enable input

*3 Chip enable input

*4 TA → PROM control signal input

* All of port options can be specified in bit unit.

* A state of pins at reset.

Pin name	Input/output mode	A state of pullup resistor specified at pullup option
Ports 0,7	Input	Fixed pullup resistor exist
Ports 1,2	Input	Programmable pullup resistor OFF
Ports 3,4,5	Input	Programmable pullup resistor OFF

Pin name	A state of P-channel transistor
S0/T0～S15/T15	P-channel transistor OFF
S16～S31	P-channel transistor OFF

1. Absolute maximum ratings / Ta = 25℃, VSS = 0 V.

Parameter		Symbol	Pins	Conditions		Limits			
					VDD[v]	min.	typ.	max.	unit
Supply voltage		VDD MAX	VDD,VDDVPP	VDD=VDDVPP		-0.3	~	+7.0	V
Input voltage		VI(1)	·Ports 71,72,73 ·Port 8 ·$\overline{RES}$			-0.3	~	VDD+0.3	
		VI(2)	VP			VDD-45	~	VDD+0.3	
Output voltage		VO(1)	·S0/T0~S15/T15 ·S16~S31			VDD-45	~	VDD+0.3	
		VO(2)	PWM1			-0.3	~	VDD+0.3	
Input/output voltage		VIO(1)	·Ports 0,1,2,70 ·Ports 3,4,5 at CMOS output			-0.3	~	VDD+0.3	
		VIO(2)	·Ports 3,4,5 at open drain output			-0.3	~	15	
High Level output current	Peak output current	IOPH(1)	·Ports 0,1,2,3,4,5 ·PWM1	·CMOS output ·At each pins.		-4			mA
		IOPH(2)	S0/T0~S15/T15	At each pins.		-30			
		IOPH(3)	S16~S31	At each pins.		-15			
	Total output current	ΣIOAH(1)	Ports 0,1,3	The total all pins.		-25			
		ΣIOAH(2)	·Ports 2,4,5 ·PWM1	The total all pins.		-25			
		ΣIOAH(3)	·S0/T0~S15/T15 ·S16~S31	The total all pins.		-140			
Low Level output current	Peak output current	IOPL(1)	Ports 0,1,2,3,4,5 ·PWM1	At each pins.				20	
		IOPL(2)	Port 70	At each pins.				15	
	Total output current	ΣIOAL(1)	Ports 0,1	The total all pins.				40	
		ΣIOAL(2)	Port 3	The total all pins.				40	
		ΣIOAL(3)	·Ports 2,5,70 ·PWM1	The total all pins.				40	
		ΣIOAL(4)	Port 4	The total all pins.				40	
Power dissipation(max.)		Pdmax	QFP100E	Ta=-30~+70℃				500	mW
Operating temperature range		Topg				-30		70	℃
Storage temperature range		Tstg				-65	~	150	

Notes · The baking must be done before mounting the QFP on the substrate (This baking is called pre-baking). After pre-baking, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30℃ or less and a humidity level of 70% or less. Please solder within eight hours.

2. Recommended operating range / Ta =-30℃ to +70℃, VSS = 0 V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[v]	min.	typ.	max.	unit.
Operating supply voltage range	VDD	VDD	0.98 μs ≦ Tcyc Tcyc ≦ 400 μs		4.5		6.0	V
HOLD voltage	VHD	VDD	RAMs and Registers hold voltage at HOLD mode.		2.0		6.0	
Pulldown voltage	VP	VP		4.5~6.0	-35		VDD	
Input high voltage	VIH(1)	Port 0 (Schmitt)	Output disable	4.5~6.0	0.4VDD +0.9		VDD	
	VIH(2)	·Ports 1,2 ·Ports 72,73 ·Ports 3,4,5 at CMOS output. (Schmitt)	Output disable	4.5~6.0	0.75VDD		VDD	
	VIH(3)	·Ports 3,4,5 at open drain output. (Schmitt)	Output disable	4.5~6.0	0.75VDD		13.5	
	VIH(4)	·Port 70 Port input/ interrupt. ·Port 71 ·$\overline{RES}$ (Schmitt)	Output N-channel Tr. OFF	4.5~6.0	0.75VDD		VDD	
	VIH(5)	Port 70 Watchdog timer.	Output N-channel Tr. OFF	4.5~6.0	0.9VDD		VDD	
	VIH(6)	Port 8		4.5~6.0	0.75VDD		VDD	
Input low voltage	VIL(1)	Port 0 (Schmitt)	Output disable	4.5~6.0	VSS		0.2VDD	
	VIL(2)	·Ports 1,2,3,4,5 ·Ports 72,73 (Schmitt)	Output disable	4.5~6.0	VSS		0.25VDD	
	VIL(3)	·Port 70 Port input/ interrupt. ·Port 71 ·$\overline{RES}$ (Schmitt)	N-channel Tr. OFF	4.5~6.0	VSS		0.25VDD	
	VIL(4)	Port 70 Watchdog timer.	N-channel Tr. OFF	4.5~6.0	VSS		0.8VDD -1.0	
	VIL(5)	Port 8		4.5~6.0	VSS		0.25VDD	
Operation cycle time	Tcyc			4.5~6.0	0.98		400	μs

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[v]	min.	typ.	max.	unit.
Oscillation frequency range (Note 1)	FmCF(1)	CF1,CF2	·12MHz(ceramic resonator oscillation). ·Refer to figure 1	4.5～6.0	11.76	12	12.24	MHz
	FmCF(2)	CF1,CF2	·3MHz(ceramic resonator oscillation). ·Refer to figure 1	4.5～6.0	2.94	3	3.06	
	FmRC		RC oscillation	4.5～6.0	0.4	0.8	2.0	
	FsXtal	XT1,XT2	·32.768kHz(crystal oscillation). ·Refer to figure 2	4.5～6.0		32.768		kHz
Oscillation stable time period (Note 1)	TmsCF(1)	CF1,CF2	·12MHz(ceramic resonator oscillation). ·Refer to figure 3	4.5～6.0		0.02	0.3	ms
	TmsCF(2)	CF1,CF2	·3MHz(ceramic resonator oscillation). ·Refer to figure 3	4.5～6.0		0.1	1	
	TssXtal	XT1,XT2	·32.768kHz(crystal oscillation). ·Refer to figure 3	4.5～6.0		1	1.5	s

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical characteristics / Ta=-30℃ to +70℃, VSS=0 V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[v]	min.	typ.	max.	unit.
Input high current	IIH(1)	·Ports 3,4,5 at open drain output	·Output disable ·VIN=13.5V (including off-leak current of output Tr.)	4.5~6.0			5	μA
	IIH(2)	·Port 0 without pullup MOS Tr. ·Potrs 1,2,3,4,5	·Output disable ·Pullup MOS Tr. OFF. VIN=VDD (including off-leak current of output Tr.)	4.5~6.0			1	
	IIH(3)	·Port 7 without pullup MOS Tr. ·Port 8	VIN=VDD	4.5~6.0			1	
	IIH(4)	·$\overline{RES}$	VIN=VDD	4.5~6.0			1	
Input low current	IIL(1)	·Ports 1,2,3,4,5 ·Port 0 without pullup MOS Tr.	·Output disable ·Pullup MOS Tr. OFF. VIN=VSS (including off-leak current of output Tr.)	4.5~6.0	-1			
	IIL(2)	·Port 7 without pullup MOS Tr. ·Port 8	VIN=VSS	4.5~6.0	-1			
	IIL(3)	·$\overline{RES}$	VIN=VSS	4.5~6.0	-1			
Output high voltage	VOH(1)	·Ports 0,1,2,3,4,5 at CMOS output ·PWM1	IOH=-1.0mA	4.5~6.0	VDD-1			V
	VOH(2)		IOH=-0.1mA	4.5~6.0	VDD-0.5			
	VOH(3)	S0/T0~S15/T15	IOH=-20mA	4.5~6.0	VDD-1.8			
	VOH(4)		·IOH=-1.0mA ·The current of any unmeasure-ment pin is not over 1 mA.	4.5~6.0	VDD-1			
	VOH(5)	S16~S31	IOH=-5mA	4.5~6.0	VDD-1.8			
	VOH(6)		·IOH=-1.0mA ·The current of any unmeasure-ment pin is not over 1 mA.	4.5~6.0	VDD-1			
Output low voltage	VOL(1)	Ports 0,1,2,3,4,5	IOL=10mA	4.5~6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5~6.0			0.4	
	VOL(3)	Port 70	IOL=1mA	4.5~6.0			0.4	
Pullup MOS Tr. resistor	Rpu	·Ports 0,1,2,3,4,5 ·Port 7	VOH=0.9 VDD	4.5~6.0	15	40	70	kΩ

Parameter	Symbol	Pins	Conditions	VDD[v]	Limits min.	typ.	max.	unit.
Output off-leakage current	IOFF(1)	·S0/T0～S6/T6 (Without pull down resistor.)	·Output P-channel Tr . OFF. ·VOUT=VSS	4.5～6.0	-1			μA
	IOFF(2)		·Output P-channel Tr . OFF. ·VOUT=VDD-40v	4.5～6.0	-30			
Pulldown transistor resistor	Rpd	·S7/T7～S15/T15 ·S16～S31 (With pulldown resistor.)	·Output P-channel Tr . OFF. ·VOUT=3V ·Vp=-30V	5.0	60	100	200	kΩ
Hysteresis voltage	VHIS	·Ports 0,1,2,3,4,5 ·Port 7 ·RES	·Output disable	4.5～6.0		0.1VDD		V
Pin capacitance	CP	All pins.	·f=1MHz ·Unmeasurement terminals for input are set to VSS level. ·Ta=25℃	4.5～6.0		10		pF

4. Serial input/output characteristics / Ta=-30℃ to +70℃, VSS = 0 V

Parameter			Symbol	Pins	Conditions	Limits				
						VDD[v]	min.	typ.	max.	unit.
Serial clock	Input clock	Cycle	TCKCY(1)	SCK0,SCK1	Refer to figure 5	4.5～6.0	2			Tcyc
		Low level pulse width	TCKL(1)			4.5～6.0	1			
		High level pulse width	TCKH(1)			4.5～6.0	1			
	Output clock	Cycle	TCKCY(2)	SCK0,SCK1	·Use pullup resistor (1kΩ) when open drain output. ·Refer to figure 5	4.5～6.0	2			
		Low level pulse width	TCKL(2)			4.5～6.0		1/2Tckcy		
		High level pulse width	TCKH(2)			4.5～6.0		1/2Tckcy		
Serial input	Data set up time		TICK	·SI0,SI1 ·SB0,SB1	·Data set-up to SCK0,1	4.5～6.0	0.1			μs
	Data hold time		TCKI		·Data hold from SCK0,1 ·Refer to figure 5	4.5～6.0	0.1			
Serial output	Output delay time (Serial clock is extrnal clock)		TCKO(1)	·SO0,SO1 ·SB0,SB1	·Use pullup resistor (1kΩ) when open drain output.	4.5～6.0			7/12Tcyc +0.2	
	Output delay time (Serial clock is internal clock)		TCKO(2)		·Data hold from SCK0,1 ·Refer to figure 5	4.5～6.0			1/3Tcyc +0.2	

5. Pulse input conditions / Ta=-30℃ to +70℃, VSS = 0 V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[v]	min.	typ.	max.	unit.
High/low level pulse width	TPIH(1) TPIL(1)	·INT0,INT1 ·INT2/T0IN	·Interrupt acceptable ·Timer0-countable	4.5～6.0	1			Tcyc
	TPIH(2) TPIL(2)	INT3/T0IN (The noise rejection clock select to 1/1.)	·Interrupt acceptable ·Timer0-countable	4.5～6.0	2			
	TPIH(3) TPIL(3)	INT3/T0IN (The noise rejection clock select to 1/64.)	·Interrupt acceptable ·Timer0-countable	4.5～6.0	128			
	TPIL(4)	$\overline{RES}$	Reset acceptable	4.5～6.0	200			μs

6. A/D converter characteristics /Ta=-30℃ to +70℃, VSS = 0 V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[v]	min.	typ.	max.	unit.
Resolution	N			4.5～6.0		8		bit
Absolute precision (Note 2)	ET			4.5～6.0			±1.5	LSB
Conversion time	TCAD		AD conversion time=16×Tcyc (ADCR2=0) (Note 3)	4.5～6.0	15.68 (Tcyc=0.98 μs)		65.28 (Tcyc=4.08 μs)	μs
			AD conversion time=32×Tcyc (ADCR2=1) (Note 3)		31.36 (Tcyc=0.98 μs)		130.56 (Tcyc=4.08 μs)	
Analog input voltage range	VAIN	AN0～AN7		4.5～6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5～6.0			1	μA
	IAINL		VAIN=VSS	4.5～6.0	-1			

(Note 2) Absolute precision excepts quantizing error(±1/2 LSB).

(Note 3) The conversion time means the time to set complete digital conversion value to register from execution of instruction to start conversion.

7.Current dissipation characteristics / Ta=-30℃ to +70℃, VSS = 0 V

Parameter	Symbol	Pins	Conditions	VDD[v]	Limits min.	typ.	max.	unit.
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD	·FmCF=12MHz Ceramic resonator oscillation. ·FsXtal=32.768 kHz crystal oscillation. ·System clock : CF oscillation. ·Internal RC oscillation stops.	4.5～6.0		11	27	mA
	IDDOP(2)		·FmCF=3MHz Ceramic resonator oscillation. ·FsXtal=32.768 kHz crystal oscillation. ·System clock : CF oscillation . ·Internal RC oscillation stops.	4.5～6.0		6	14	
	IDDOP(3)		·FmCF=0Hz (when oscillation stops). ·FsXtal=32.768 kHz crystal oscillation. ·System clock : RC oscillation.	4.5～6.0		4	12	
	IDDOP(4)		·FmCF=0Hz (when oscillation stops). ·FsXtal=32.768 kHz crystal oscillation. ·System clock : Xtal oscillation. ·Internal RC oscillation stops.	4.5～6.0		3	10	

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[v]	min.	typ.	max.	unit.
Current dissipation HALT mode (Note 4)	IDDHALT(1)	VDD	·HALT mode ·FmCF=12MHz Ceramic resonator oscillation. ·FsXtal=32.768 kHz crystal oscillation. ·System clock : CF oscillation . ·Internal RC oscillation stops.	4.5~6.0		5	10	mA
	IDDHALT(2)		·HALT mode FmCF=3MHz Ceramic resonator oscillation. ·FsXtal=32.768 kHz crystal oscillation. ·System clock : CF oscillation . ·Internal RC oscillation stops.	4.5~6.0		1.9	4.8	
	IDDHALT(3)		·HALT mode FmCF=0Hz (when oscillation stops). ·FsXtal=32.768 kHz crystal oscillation. ·System clock : RC oscillation.	4.5~6.0		400	800	μA
	IDDHALT(4)		·HALT mode FmCF=0Hz (when oscillation stops). ·FsXtal=32.768 kHz crystal oscillation. ·System clock : Xtal oscillation. ·Internal RC oscillation stops.	4.5~6.0		20	70	
Current dissipation HOLD mode (Note 4)	IDDHOLD(1)	VDD	HOLD mode	4.5~6.0		0.05	30	
	IDDHOLD(2)			2.5~4.5		0.02	20	

(Note 4) The currents of output transistors and pull-up transistors are ignored.

Table 1. Ceramic resonator oscillation guaranteed constant (main-clock)

A kind of oscillation	Producer	Oscillator	C1	C2
12MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33pF	33pF
		CSA12.0MT	33pF	33pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	33pF	33pF
3MHz ceramic resonator oscillation	Murata	CSA3.00MG	33pF	33pF
		CST3.00MGW	on chip	
	Kyocera	KBR-3.0MS	47pF	47pF

* Both C1 and C2 must be used K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub-clock)

A kind of oscillation	Producer	Oscillator	C3	C4
32.768kHz crystal oscillation	Dai Sinku	DT-38(1TA252E00)	18pF	18pF
	Kyocera	KF-38G-13P0200	18pF	18pF

* Both C3 and C4 must be used J rank (±5%) and CH characteristics.
(Not in need of high precision, use K rank (±10%) and SL characteristics.)

Notes ·Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
·If you use other oscillators herein, we provide no guarantee for the characteristics.

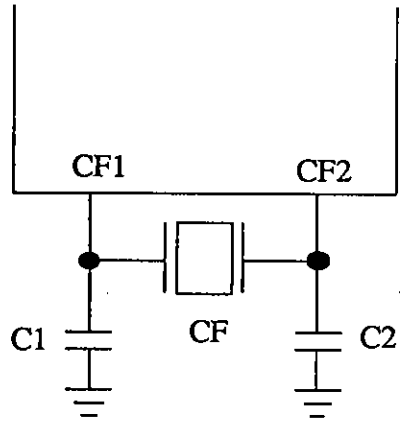


Figure 1 Main-clock circuit
Ceramic resonator oscillation

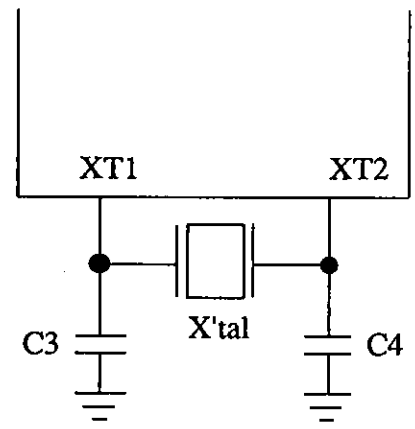


Figure 2 Sub-clock circuit
Crystal oscillation

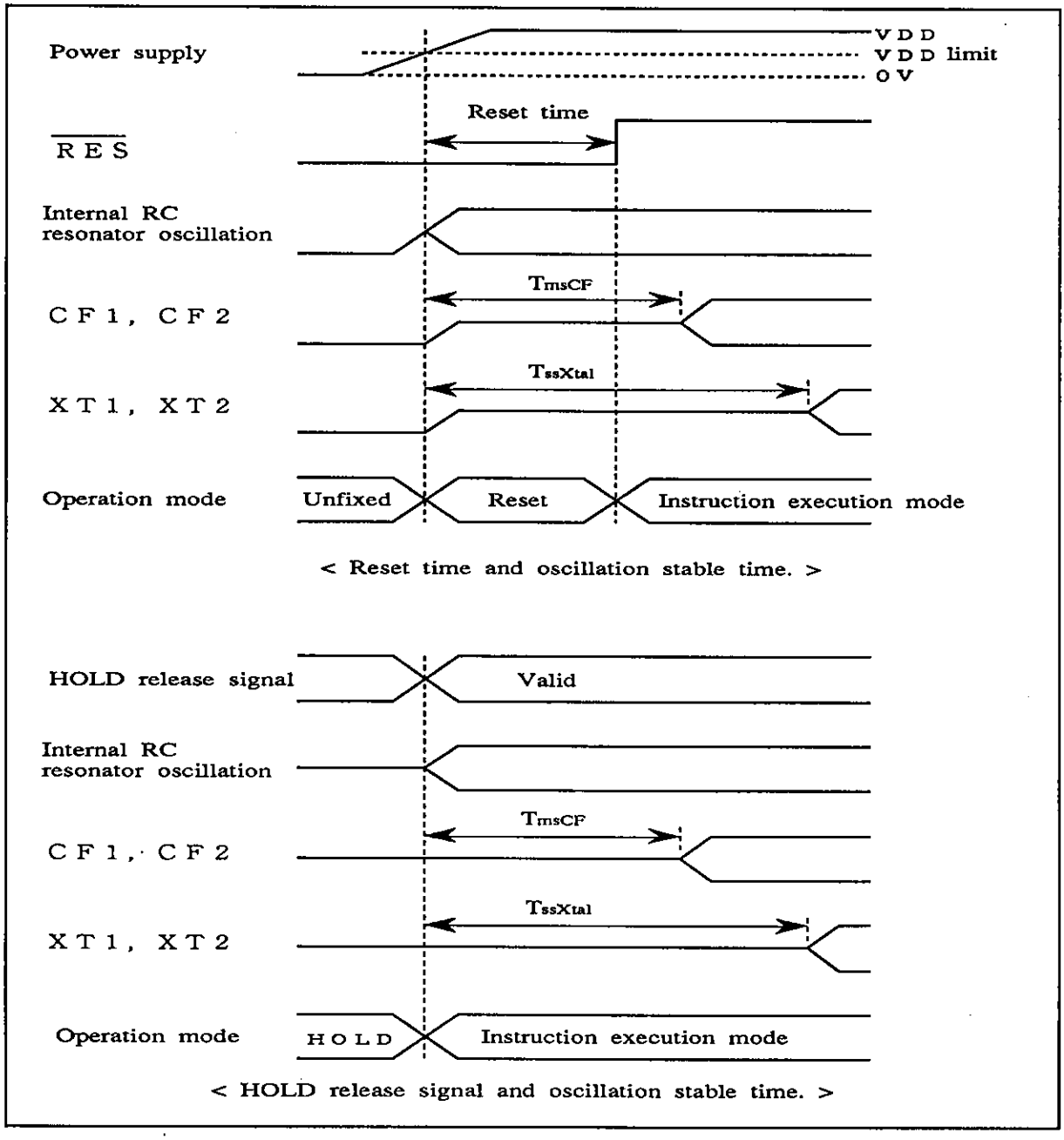
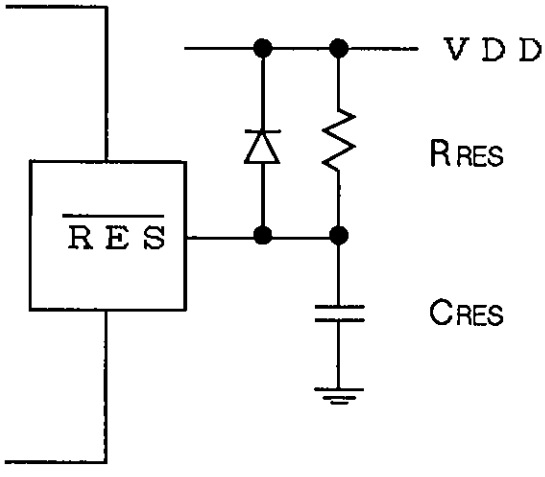
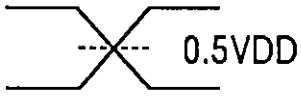


Figure.3 Oscillation stable time

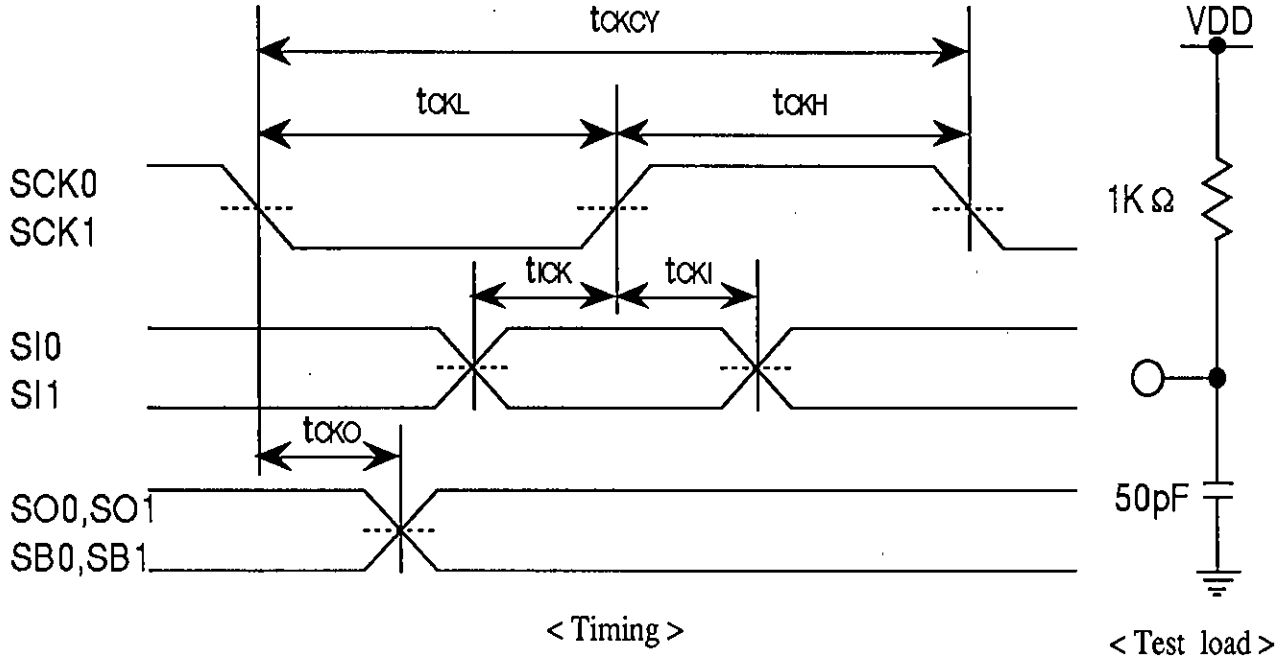


(Note) Fix the value of CRES, RRES that is sure to reset untill 200μs, after Power supply has been over inferior limit of supply voltage.

Figure. 4 Reset circuit.



< AC timing point >



< Timing >

< Test load >

Figure. 5 Serial input/output test condition.

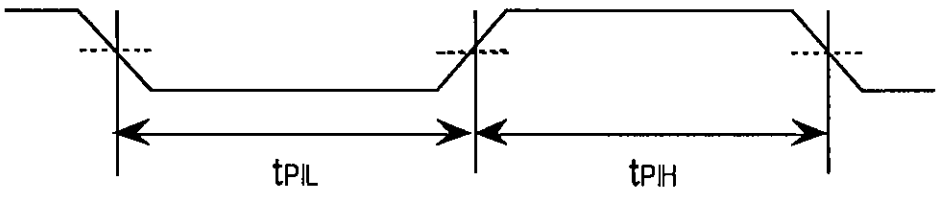


Figure. 6 Pulse input timing condition.